

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on April 11, 2007.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Eric Robinson on May 15, 2008.

The application has been amended as follows:

In Claim 17, amend the claim so that it reads:

17. (Currently Amended) An electronic device comprising:

a printed wiring board;

a first wiring layer and a second wiring layer over on the printed wiring board;

a first semiconductor element using a crystalline semiconductor film as a first active region and a second semiconductor element using an amorphous semiconductor film as a second active region over an adhesive;

a third wiring layer connecting the first semiconductor element and electrically connecting to the first wiring layer; and

a fourth wiring layer connecting the second semiconductor element and electrically connecting to the second wiring layer;

wherein the amorphous semiconductor film is located above the crystalline semiconductor film.

Claim 18, amend the claim so that it reads:

18. (Currently Amended) An electronic device comprising:

a printed wiring board;

a first wiring layer and a second wiring layer ~~over~~ on the printed wiring board;

a first semiconductor element using a crystalline semiconductor film as a first active region and a second semiconductor element using an amorphous semiconductor film as a second active region over a plastic substrate;

a third wiring layer connecting the first semiconductor element and electrically connecting to the first wiring layer; and

a fourth wiring layer connecting the second semiconductor element and electrically connecting to the second wiring layer;

wherein the amorphous semiconductor film is located above the crystalline semiconductor film.

Claim 19, amend the claim so that it reads:

19. (Currently Amended) An electronic device comprising:

a printed wiring board;

a first wiring layer and a second wiring ~~layer-over~~ on the printed wiring board;

a first semiconductor element using a crystalline semiconductor film as a first active region and a second semiconductor element using an amorphous semiconductor film as a second active region over an adhesive;

a third wiring layer connecting the first semiconductor element and electrically connecting to the first wiring layer; and

a fourth wiring layer connecting the second semiconductor element and electrically connecting to the second wiring layer;

wherein the first semiconductor element and the second semiconductor element are electrically connected to each other, and

wherein the amorphous semiconductor film is located above the crystalline semiconductor film.

Claim 20, amend the claim so that it reads:

20. (Currently Amended) An electronic device comprising:

a printed wiring board;

a first wiring layer and a second wiring layer ~~over~~ on the printed wiring board;

a first semiconductor element using a crystalline semiconductor film as a first active region and a second semiconductor element using an amorphous semiconductor film as a second active region over a plastic substrate;

a third wiring layer connecting the first semiconductor element and electrically connecting to the first wiring layer; and

a fourth wiring layer connecting the second semiconductor element and electrically connecting to the second wiring layer;

wherein the first semiconductor element and the second semiconductor element are electrically connected to each other, and

wherein the amorphous semiconductor film is located above the crystalline semiconductor film.

Claim 25, amend the claim so that it reads:

25. (Currently Amended) An electronic device comprising:

a controller over a printed wiring board;

a power supply circuit over the printed wiring board;

a first wiring layer and a second wiring layer ~~over~~ on the printed wiring board;

an optical sensor over the printed wiring board comprising a first semiconductor element using a crystalline semiconductor film as a first active region and a second semiconductor element using an amorphous semiconductor film as a second active region over a plastic substrate;

a third wiring layer connecting the first semiconductor element and electrically connecting to the first wiring layer; and a fourth wiring layer connecting the second semiconductor element and electrically connecting to the second wiring layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew E Warren/
Primary Examiner, Art Unit 2815

May 16, 2008